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SEEDLESS WIREBOND PAD PLATING

Abstract

An integrated circuit (IC) chip, semiconductor wafer with IC chips in a number of die locations and a method of making the IC chips on the wafer. The IC chips have plated chip interconnect pads. Each plated pad includes a noble metal plated layer electroplated to a platable metal layer. The platable metal layer may be copper and the noble metal plated layer may be of gold, platinum, palladium, rhodium, ruthenium, osmium, iridium or indium.